# AN14390

## MCXA14x/15x ADC的使用和计算工具

第1.0版—2024年10月16日

应用笔记

**文档信息**

| 信息 | 内容 |
|---|---|
| 关键词 | AN14390、ADC的使用和计算工具、MCXA14x、MCXA15x |
| 摘要 | 本文档介绍了MCXA芯片提供的ADC功能和附带的Excel电子表格计算工具。 |

# 1 介绍

本文档介绍了MCXA芯片的模数转换器（ADC）功能和Excel电子表格计算工具，这些功能可以计算采样时间和源阻抗，帮助用户为特定应用程序选取适当的参数。

***注：**要计算采样时间或源阻抗，请参阅**ADC_Specs_Calculator_MCXA.xlsx**。*

MCX A14x/A15x Arm Cortex-M33通用MCU的工作频率最高为96MHz，具有高集成度和强大的模拟能力，提供多种低功耗智能外设，其中包括具有硬件平均功能的4Msps 12位ADC。

# 2 MCXA的ADC功能

ADC模块在MCXA1x2/1x3器件上有一个模块`ADC0`，在MCXA1x4/1x5/1x6器件上有两个模块`ADC0`和`ADC1`，具有以下功能：

- 线性逐次逼近算法
- 16位或12位分辨率的单端操作
- 支持4个带优先级配置的硬件触发源，和8条结果先进先出（FIFO）的缓存器
- 7个命令缓冲区，允许独立选择选项和通道序列扫描
- 8条转换结果数据先进先出（FIFO）缓存器，带可配置的水印标记和溢出检测功能
- 带“*为真时存储*”和“*重复直至为真*”选项的比较功能
- 可配置的模拟输入采样时间
- 可配置的速率选项，以适应SoC的低功耗模式下的操作
- 中断、直接内存访问（DMA）或轮询操作
- 线性度和增益调整校准逻辑

MCXA上有多种低功耗模式。ADC模块在不同功耗模式下的状态如表1所示。

**表1. ADC在不同功耗模式下的状态**

| 模块 | 功耗模式 | | | |
| --- | --- | --- | --- | --- |
| | 睡眠 | 深度睡眠 | 掉电 | 深度掉电 |
| ADC的数字部分 | ON | 静态/LP | 静态 | OFF |
| ADC的模拟部分 | ON/OFF | ON/OFF | 静态 | OFF |

**ON**：正常工作。
**OFF**：该部分断电，所有电气信息丢失。
**ON/OFF**：工作在ON或OFF状态，由此外设的配置控制。
**LP**：LP模块处于低功耗状态（时钟门控、异步操作等）。对于数字模块，它可以通过异步功能时钟来激活。
**Static（静态）**：该部分不可读/写或修改，但数据会保留。

# 3 ADC的运行

本节提供了有关ADC时钟源、参考电压源、触发信号、CMD配置、比较功能和校准的信息。


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## 3.1 ADC的时钟源

在中等驱动（MD）模式下，ADC的最大频率为24MHz，其中VDD_CORE为1.0V，而在标准驱动（SD）模式下，ADC的最大频率为64MHz，其中VDD_CORE为1.1V。ADC有4个时钟源和一个4位时钟分频器，如图1所示。

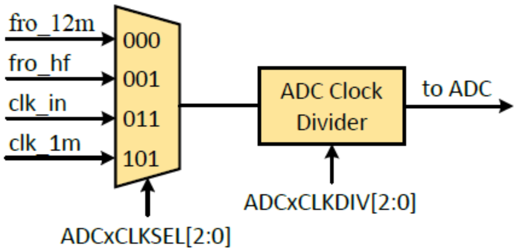


**图1. ADC的时钟源和分频器**

其中：

- fro_12m：来自FRO12M的12MHz时钟输出
- fro_hf：来自 FRO192M的时钟输出（频率由SCG_FIRCCFG[FREQ_SEL]控制）
- clk_in：来自外部振荡器的内部时钟
- clk_1m：来自FRO12M的1MHz时钟输出
- DIV+1：分频器值

## 3.2 ADC的参考电压源

ADC的参考电压可以通过CFG[REFSEL]选择，如下所示：

- CFG[REFSEL]=00，VREFH参考引脚
- CFG[REFSEL]=01，VREFI
- CFG[REFSEL]=10，VDDA_ANA电源引脚

## 3.3 ADC的触发源

一个ADC模块有4个硬件触发源。触发源可以在INPUTMUX中选择。INPUTMUX为内部外设提供信号连通选项。一些外设输入可被复用至多个输入源。这些源可以是外部引脚、中断、其它外设的输出信号或其它内部信号。有关详细的触发源列表和相应的多路复用器排序号，请参阅《MCX A153/A152/A143/A142参考手册》（文档MCXAP64M96FS3RM）和《MCXA156/A155/A154/A146/A145/A144参考手册》（文档MCXAP100M96FS6RM）的“输入多路复用（INPUTMUX）”寄存器描述的“ADC触发输入连接（ADCxTRIG0-ADCxTRIG3）”章节。

ADC命令CMD1-CMD7的执行由触发信号发起。每个触发信号都可以通过设置相应的SWTRIG[SWTn]位域由软件生成。或者，也可以从模块外围的异步输入源生成硬件触发信号。例如，要定期触发转换，可以使用脉宽调制（PWM）信号。当启用硬件触发输入时，会在相关硬件触发源的上升沿上检测到硬件触发事件。每个触发源都会通过对应的优先级控制字段（TCTRLa[TPRI]）分配一个优先级。每个触发源都通过对应的命令选择字段（TCTRLa[TCMD]）与命令缓冲区相关联。


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## 3.4 ADC的CMD

ADC根据CMD配置执行转换，并加载下一个CMD或恢复到空闲状态。CMD可以由来自INPUTMUX的硬件触发信号触发，或通过软件触发信号触发。转换结果与相应的CMD配置一起存储在结果FIFO中。

详细的ADC转换操作可以在CMD寄存器中配置：

- `CMDLx[MODE]`：选择转换的分辨率。
- `CMDLx[ADCH]`：选择输入通道。
- `CMDHx[NEXT]`：选择要执行的下一个CMD。如果该区域为`0`，则ADC将返回空闲状态，并等待下一个触发事件。
- `CMDHx[LOOP]`：选择此命令重复执行的次数。该命令执行`LOOP+1`次，每次都将结果存储在FIFO中。
- `CMDHx[AVGS]`：选择对多少次ADC转换进行平均以创建一个结果。转换执行2AVGS次，但FIFO中仅存储一个平均结果。
- `CMDHx[STS]`：选择采样时间。如果STS=0，则最小采样时间为3.5个ADCK周期。总采样时间为（3.5+2STS）个ADCK周期，STS应为一个非零值。
- `CMDHx[LWI]`：如果此位被置位，则在下一个循环中执行命令时必须递增输入通道。
- `CMDHx[WAIT_TRIG]`：如果此位被置位，则当前命令指向的下一个命令就无法执行，直到有效的触发信号再次被发出。
- `CMDHx[CMPEN]`：配置比较功能。当`CMPEN=10b`时，比较功能启用且当比较结果为真（true）时将ADC结果存储在FIFO中。无论比较结果如何，在执行命令后循环计数都会增加。当`CMPEN=11b`时，重复执行该命令，直至比较结果为真（true）。

## 3.5 比较功能

每个对应的命令有7个比较值寄存器`CV1-CV7`。每个`CV`寄存器可分成两个16位区域，即“低比较值”（CVL）和“高比较值”（CVH）。如果转换结果大于CVH或小于CVL，则比较结果为真（true）。

## 3.6 ADC校准

ADC模块具有偏移校准和ADC校准功能，这些功能必须在ADC初始化时执行，以实现更高的精度。校准必须在每次复位后和执行转换之前进行。

在校准过程中，对多次转换进行平均可以提高精度。建议在校准过程中将`CTRL[CAL_AVGS]`设置为至少256次平均。

偏移调整寄存器（OFSTRIM）用于对ADC比较器的偏移电压进行调整。ADC支持偏移校准功能，其中OFSTRIM寄存器会自动更新。通过设置`CTRL[CALOFS]`发起偏移校准。轮询`STAT[CAL_RDY]`标志位。当`STAT[CAL_RDY]`置位时，偏移校准功能已完成，OFSTRIM寄存器被更新。

ADC包含一个硬件校准逻辑，用于对转换器进行校准，以校正原始转换结果的增益误差和线性误差。ADC支持校准功能，其中`CAL_GAR`寄存器会自动更新。校准功能还会更新`GCC0[GAIN_CAL]`。需要软件计算才能从`GCC0[GAIN_CAL]`中推导出`GCR0[GCALR]`。

以下是完成校准设置的步骤：


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1. 执行偏移校准步骤。OFSTRIM在校准期间用于调整比较器偏移电压。
2. 通过向CTRL[CAL_REQ]中写入1来启动校准例程。
   a. CTRL[CAL_REQ]保持为1，直至CAL例程被ADC接受。
   b. 接受后，CTRL[CAL_REQ]自动变为0。
3. 轮询GCR0[RDY]标志位。
   当该标志位被置位时，硬件控制的校准操作已完成，且CAL_GAR和GCC0[GAIN_CAL]寄存器已被更新。需要GCC0[GAIN_CAL]中的更新值，用于以下步骤中描述的后续软件处理。
4. 读取GCC0[GAIN_CAL]并存储，以用于增益调整计算。
5. 计算增益调整 = (131072)/(131072-GCC0[GAIN_CAL])。GCC0[GAIN_CAL]是一个16位有符号值。
   a. 这些结果是一个介于0和2之间的浮点值。
6. 将该浮点值转换为整数部分（0或1），并将其小数部分四舍五入为16位数。
   a. 将整数值存储到GCR0[GCALR[16]]中。
   b. 将小数部分存储到GCR0[GCALR[15:0]]中。
   c. 将此值写入到GCR0[GCALR]寄存器中。
7. 一旦GCR0[GCALR]包含了增益调整计算的结果，对GCR0[RDY]标志位进行置位，以指示其是有效的。

完成上述步骤后，校准过程完成，STAT[CAL_RDY]标志位被置位。STAT[CAL_RDY]标志位将保持置位状态，直到用户重置系统或请求一个新的校准过程。

当STAT[CAL_RDY]被置位时，ADC配置为在校准模式下运行。每次转换都使用线性度和增益校准结果的组合来校正逐次逼近寄存器（SAR）的数据。处理每个样本都需要校准转换延迟。然而，由于数据和控制过程的流水线性质，每次转换仍然可以在不进行这种校准延迟的情况下启动。

## 4 ADC计算工具

ADC计算工具的目的是根据输入信号的阻抗特性来确定可以实现的最大采样率。为了准确地采样输入电压，必须合适地选择源电阻和ADC采样时间。ADC的简化电路如图2所示。


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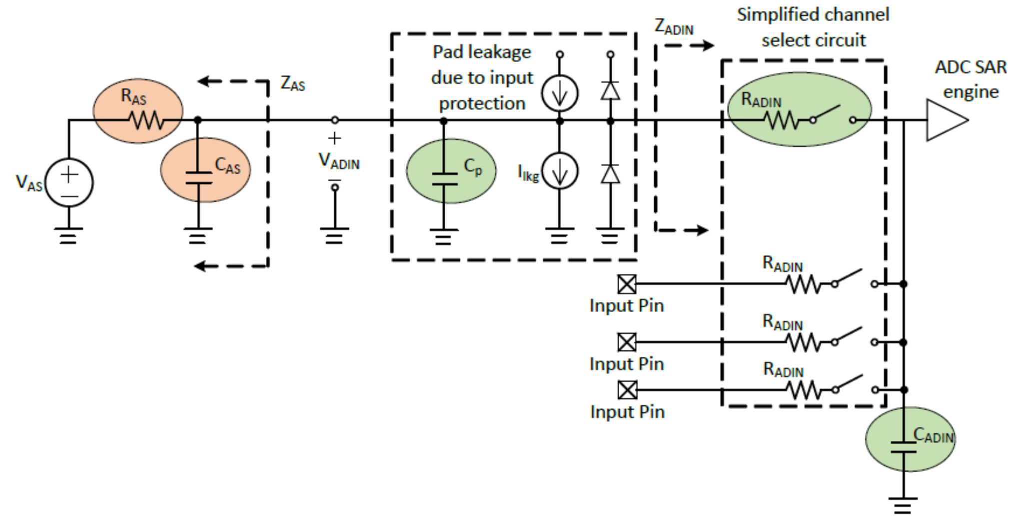


**图2. ADC的简化电路图**

公式1给出了对于一个固定源电阻（$R_{AS}$）所需的采样时间：

$$T_{SMP_{REQ}} = B \cdot \ln(2) \cdot \left[R_{AS} \cdot (C_{AS} + C_P + C_{ADIN}) + (R_{AS} + R_{ADIN})C_{ADIN}\right] \quad (1)$$

其中：

- B：期望精度（位）
- $C_{AS}$：源电容
- $C_P$：管脚/封装的寄生电容
- $C_{ADIN}$：输入电容
- $R_{ADIN}$：输入电阻

实际采样时间由ADC命令寄存器中的“ADC输入时钟频率”（$F_{ADCLK}$）和“采样时间选择”（STS）位决定，这些位可决定采样周期数，见公式2：

$$T_{SMP} = \frac{CYC_{SMP}}{F_{ADCLK}} \quad (2)$$

$CYC_{SMP}$可编程为3.5至131.5个周期。$T_{SMP}$必须配置为大于或等于$T_{SAM_REQ}$。如果设置$T_{SMP} > T_{SMP_REQ}$并求解$R_{AS}$，则可以得到允许以期望精度进行采样的最大源电阻：

$$R_{AS} < \frac{\frac{CYC_{SMP}}{F_{ADCLK} \cdot B \ln(2)} - R_{ADIN} \cdot C_{ADIN}}{C_{AS} + C_P + 2 \cdot C_{ADIN}} \quad (3)$$

公式3假设输入电压在后续的转换之间可以变化至满量程（$V_{refh}$-$V_{refl}$）。如果后续转换之间的最大输入电压变化已知且小于$V_{refh}$-$V_{refl}$，则可以调整B的值。例如，要在12位时获得1/2 LSB的采样精度，如果已知最大输入电压变化仅为（$V_{refh}$-$V_{refl}$）/4，则设置B=11而非13。

图3所示为此工具的第一部分，此部分指定了一个固定$R_{AS}$所需的采样时间。用户可以输入源电阻$R_{AS}$、源电容$C_{AS}$（均为外部元件）、分辨率B和ADC可接受的采样误差精度修正值。



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| To calculate the required sample time given fixed $R_{AS}$ | | |
|---|---|---|
| **Input (Enter value in yellow highlighted cells)** | | |
| $R_{AS}$ | 100 | Ω |
| $C_{AS}$ | 100.00 | pF |
| Resolution | 12 | bits |
| Accuracy Modifier | 1 | bits |
| B | 10 | bits |
| $C_P$ | 3.00 | pF |
| $C_{ADIN}$ | 1.92 | pF |

| **Output** | | |
|---|---|---|
| **Direct input channel** | **$R_{ADIN}$ (kΩ)** | **$T_{SMP\_REQ}$ (ns)** |
| $V_{DDA}$>1.8 | 1.65 | 96.01 |
| $V_{DDA}$>3.0 | 1.35 | 92.02 |
| **Muxed input channel** | **$R_{ADIN}$ (kΩ)** | **$T_{SMP\_REQ}$ (ns)** |
| $V_{DDA}$>1.8 | 7.00 | 200.66 |
| $V_{DDA}$>3.0 | 2.01 | 120.97 |

**图3. ADC所需采样时间的计算工具**

图4所示为该工具的第二部分，根据采样时间和所使用的ADC频率提供最大源电阻。在第一部分中，用户可以根据正在使用的参数更改黄色突出显示的单元格。检查$CYC_{SMP_USED}$是否大于$CYC_{MIN}$。然后可以生成最大的源电阻和转换率。用户可以利用这些数据来设计一个采样电路，并用合适的参数对ADC进行初始化。

| To calculate maximum $R_{AS}$ with given sample time and ADC input clock frequency | | | | |
|---|---|---|---|---|
| **Input (Enter value in yellow highlighted cells)** | | | | |
| Resolution | 12 | bits | CMDH[STS] | 100 |
| $C_{AS}$ | 100.00 | pF | CMDH[AVGS] | 0000 |
| ADCnCLKDIV[DIV] | 1 | | CFG2[HS] | 1 |
| Accuracy Modifier | -1 | bits | CFG2[HSEXTRA] | 0 |
| B | 10 | bits | CFG2[TUNE] | 01 |
| ADC clock source frequency | 96 | MHz | CMDLa[MODE] | 0 |
| $F_{ADCK}$ | 48 | MHz | ADCK cycles/conversion | 35.5 |
| $C_P$ | 3.00 | pF | | |
| $C_{ADIN}$ | 4.00 | pF | | |

| **Output** | | | | | | |
|---|---|---|---|---|---|---|
| **Direct input channel** | **$R_{ADIN}$ (kΩ)** | **$CYC_{SMP\_MIN}$** | **$CYC_{SMP\_USER}$** | **$T_{SMP}$ (ns)** | **$R_{AS\_MAX}$ (Ω)** | **ADC sampling frequency (Msamples/s)** |
| $V_{DDA}$>1.8 | 1.65 | 4.6 | 19.5 | 406.25 | 468.55 | 1.35 |
| $V_{DDA}$>2.1 | 1.35 | 4.4 | 19.5 | 406.25 | 479.36 | 1.35 |
| **Muxed input channel** | **$R_{ADIN}$ (kΩ)** | **$CYC_{SMP\_MIN}$** | **$CYC_{SMP\_USER}$** | **$T_{SMP}$ (ns)** | **$R_{AS\_MAX}$ (Ω)** | **ADC sampling frequency (Msamples/s)** |
| $V_{DDA}$>1.8 | 7.00 | 9.6 | 19.5 | 406.25 | 275.76 | 1.35 |
| $V_{DDA}$>2.1 | 2.01 | 5.8 | 19.5 | 406.25 | 455.58 | 1.35 |

**图4. ADC的采样频率和RAS计算工具**

计算工具中的其它参数如下：

- $f_{ADCK}$：输入时钟频率
- $CYC_{SMP\_MIN}$：$T_{SMP}$ > $T_{SMP_REQ}$时所需的最小采样周期



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- $CYC_{SMP\_USER}$：用户使用`CMDHn[STS]`设置的采样周期
- $T_{SMP}$：用户设置的采样时间

## 5 参考资料

表2列出了可以参考以获取更多信息的其它文档和资源。下面列出的一些文档可能仅在保密协议（NDA）下才能获得。要请求访问这些文档，请联系当地的现场应用工程师（FAE）或销售代表。

**表2. 相关文档/资源**

| 文档 | 链接/如何访问 |
| --- | --- |
| 《MCX A153/A152/A143/A142参考手册》 | MCXAP64M96FS3RM |
| MCUXpresso SDK (SDK_2.14.2_FRDM-MCXA153) | MCUXpresso SDK |
| 《MCXA156/A155/A154/A146/A145/A144参考手册》 | MCXAP100M96FS6RM |

## 6 修订历史

表3汇总了本文档的修订情况。

**表3. 修订历史**

| 文档ID | 发布日期 | 说明 |
| --- | --- | --- |
| AN14390 v.1.0 | 2024年10月16日 | 首次公开发布 |


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